REMARKS

Dependent claim 9 is amended for purposes of clarification with an example embodiment shown on page 10, line 23 of the specification. Claims 1-2 and 5-10, and 13-18 remain for consideration and are thought to be in condition for allowance. Reconsideration and allowance are respectfully requested.

The Office Action does not establish that claims 1-2, 5, 13-14 and 18 are unpatentable under 35 USC §103(a) over "Seeley" (U.S. Patent No. 6,097,429 to Seeley et al.) in view of "Filor" (U.S. Patent No. 5,844,609 to Filor et al.), "Walker" (U.S. Patent No. 6,222,881 to Walker), and "Elswick" (U.S. Patent No. 6,791,620 to Elswick et al.). The rejection is respectfully traversed because the Office Action does not show that all the limitations are suggested by the references and does not provide sufficient motivations for making the combination.

The limitations added to claim 1 in the previous amendment are not shown to be suggested by the Seeley-Filor-Walker-Elswick combination. The limitations set forth that in the second operating mode, a first data router processes a first half of the pixel data of a frame and a second data router processes a second half of the pixel data of the frame. Elswick does not suggest two routers processing the same frame. Rather Elswick teaches that "frames from the input video signal can be written to a bank of frame buffers, each buffer being operated on by a different processor..." (col. 17, l. 33-35) Thus, Elswick clearly does not have two processors operating on the same frame, and does not suggest a first data router processing a first half of a frame and a second router processing a second half of the frame.

Furthermore, the claimed data routers are configurable for operation in a first mode or a second mode, and there is no apparent suggestion of such configurability. In the first mode, a single data router processes video data from a single channel of video data while operating in the first mode, and in the second mode a first data router processes a first half of the pixel data of a frame and a second data router processes a second half of the pixel data of the frame. Neither Elswick nor the Seeley-Filor combination suggest any such configurability. Seeley teaches a single processor

performing compression (not the claimed conversion of the data routers), and the cited teachings of Elswick suggest that parallel processing may be required for processing full motion video signals. There is no suggestion of a system that is configurable to operate in a selected one of the two claimed modes. Rather, the cited art teaches either a system with a single processor or a system with parallel processors. Thus, the configurable data routers are not shown to be suggested.

The limitations of the selector circuit are not shown to be suggested by the Seeley-Filor-Walker-Elswick combination. The limitations specify that the selector circuit is configured and arranged to select digital video data received at a first data rate from a subset of the channels responsive to an input selection signal from the processor and provide selected digital video data at the output ports at a second data rate that is half the first data rate. Thus, the output (second) data rate of the selector circuit is half the input (first) data rate to the selector circuit.

Walker is not shown to suggest these limitations since Walker's target bit rate does not correspond to the claimed input data rate. Walker teaches that "The quantization tables were designed such that the finest quantization (i.e., Table 15) is at the level of visual perception and the i.e., Table 0) produces encoded signals at half the target bit rate." (col. 37, l. 64-67). Even with the apparent typographical errors in the Walker patent, it can be seen that Walker's target bit rate is not shown to correspond to the claimed input bit rate. Walker explains in col. 7, l. 30-35 that the target bit rate is the bit rate produced by a table having an index of 8. Thus, the target bit rate is an output and does not reasonably correspond to the input first data rate.

The alleged motivations combining Walker, Elswick, and Filor with Seeley are simply a hindsight reconstruction of the invention. Combining prior art references without evidence of such a suggestion, teaching, or motivation simply takes the inventor's disclosure as a blueprint for piecing together the prior art to defeat patentability—the essence of hindsight. *See, e.g., Interconnect Planning Corp v. Feil*, 774 F.2d 1132, 1138, 227 USPQ 543, 547 (Fed. Cir. 1985) ("The invention must be viewed not with the blueprint drawn by the inventor, but in the state of the art that existed at the time."). *Id.* Because the Office Action does not present evidence in

support of a motivation for combining the references, Applicant respectfully submits that that the alleged motivations are improper.

Claims 2 and 5 depend from claim 1, independent method claim 13 and independent apparatus claim 18 include limitations similar to those of claim 1, and claim 14 depends from claim 13. These claims are not shown to be unpatentable for at least the reasons set forth above.

The rejection of claims 1-5, 13-14 and 18 over the Seeley-Filor combination should be withdrawn because a *prima facie* case of obviousness has not been established.

The Office Action does not establish that claims 6-10 and 15-17 are unpatentable under 35 USC §103(a) over the Seeley-Filor combination, and further view of "Voit" (U.S. Patent No. 5,751,707 to Voit et al.). The rejection is respectfully traversed because the Office Action fails to show that all the limitations are suggested by the references.

Claim 6 depends from claim 1 and claim 8 depends from claim 6, and the limitations are not shown to be suggested for at least the reasons set forth above.

Claim 7 includes limitations of first-level priority graphics data that takes precedence for display over the graphics data of the first memory and over the video data. These limitations are not shown to be suggested by Voit. The cited teachings of Voit suggest "five different planes of video information, four of which can be active at any one time, to produce the composite video frame output signals. The individual planes comprise the decoded MPEG video frames, a cursor, two graphics/text image planes manipulated by the microprocessor 110 and a backdrop plane." The combining of the planes does not suggest any priority of the graphics data relative to other graphics data.

Furthermore, the Official Notice of prioritization as applied to the limitations of claim 7 is improper. The Office Action states that "it is notoriously well known in the art to prioritize elements of a process in the case of conflicting resource needs for the purpose of ensuring that at least the most important elements are successfully processed." The Official Notice is insufficient because it is no more than a

generalization of the concept of prioritization. This approach is improper because the approach could be used to show that all claims in all patents are suggested by what is generally known. There is no specific factual evidence presented to suggest the specific manner in which prioritization is applied in the current claim limitations.

Applicants maintain that the prior art has not been shown to suggest to sequence output of data from the first and second memories to the pixel selector and sequence first-level priority graphics data from the third memory to the digital-to-analog converter, wherein the first-level priority graphics data which takes precedence for display over the graphics data of the first memory and over the video data. If the rejection is maintained, Applicants respectfully request citation to prior art so that the manner can be further addressed.

The alleged motivation for combining Voit with the Seeley-Filor combination is improper because no specific evidence has been presented to support making the combination.

The amendment to claim 9 clarifies that the blink translation alternates between the input pixel value and the configurable pixel value at the configurable interval and causes selected graphics data to flash on a video display terminal. By including the blink function in the translation path, selected graphics data can be flashed on the video display without requiring periodic update of the VRAMS 220 and 222. This saves computation resources of processor 212 (spec. p. 11, l. 1-3).

Claim 10 includes limitations similar to those of claim 2 and is not shown to be unpatentable for at least the reasons set forth above.

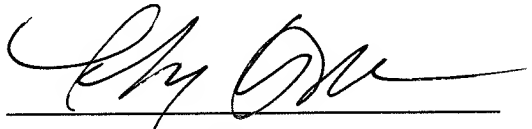
Claims 14-17 include limitations similar to those discussed above for claims 6-9. Therefore, claims 14-17 are not shown to be unpatentable for at least the reasons set forth above.

The rejection of claims 6-12 and 15-17 over the Seeley-Filor-Voit combination should be withdrawn because the Office Action fails to show all the limitations are suggested by the combination and fails to provide a proper motivation for combining the references.

Withdrawal of the rejections and reconsideration of the claims are respectfully requested in view of the remarks set forth above. No extension of time is believed to be necessary for consideration of this response. However, if an extension of time is required, please consider this a petition for a sufficient number of months for consideration of this response. If there are any additional fees in connection with this response, please charge Deposit Account No. 50-0996 (LMCO.004PA).

Respectfully submitted,

CRAWFORD MAUNU PLLC
1270 Northland Drive, Suite 390
Saint Paul, MN 55120
(651) 686-6633

By: 
Name: LeRoy D. Maunu
Reg. No.: 35,274